In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

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1. (Currently Amended) A digital system comprising a microprocessor having an instruction execution pipeline with a plurality of pipeline phases, wherein the microprocessor comprises:

program fetch circuitry operable to perform a first portion of the plurality of pipeline phases;

instruction decode circuitry connected to receive fetched instructions from the program fetch circuitry, the instruction decode circuitry operable to perform a second portion of the plurality of pipeline phases; and

at least a first functional unit connected to receive a plurality of control signals from the instruction decode circuitry, the functional unit operable to perform a third portion of the plurality of pipeline phases, the third portion being execution phases, wherein the first functional unit comprises:

first test circuitry connected to receive an operand from a selected test register, and having an output for indicating a condition of the operand;

decrement circuitry connected to receive the operand from the selected test register, and having an output connected to conditionally provide a decremented value of the operand to the test register dependent upon said indicated condition of the operand;

adder circuitry connected to receive a program counter value and a displacement value, and having an output connected to conditionally provide a branch address to a program counter register dependent upon said indicated condition of the operand; and

A15 wherein the first test circuitry, the decrement circuitry, and the adder circuitry are all operable to test the operand, conditionally decrement the operand, and conditionally provide a branch address to the program counter in response to a single conditional branch-decrement instruction ~~of a first type~~.

2. (Currently Amended) The digital system of Claim 1, wherein the first test circuitry, the decrement circuitry, and the adder circuitry are all operable to test the operand, conditionally decrement the operand, and conditionally provide a branch address to the program counter in response to a single conditional branch-decrement instruction during a single one of the third portion of pipeline phases.

3. (Canceled)

4. (Original) The digital system of Claim 3, further comprising second test circuitry connected to test a condition of a selected predicate register, and having an output for indicating a condition of the predicate register, wherein the second test circuitry is operable to inhibit the program counter from receiving the branch address if the contents of the predicate register do not correspond to a second condition.

Claims 5 to 9. (Canceled)

10. (Currently Amended) A method of operating a digital system having a microprocessor with a conditional ~~branch~~ branch-decrement instruction, comprising the steps of:

fetching a conditional ~~branch~~ branch-decrement instruction for execution;

testing a test register selected by the conditional ~~branch~~ branch-decrement instruction to determine if the contents of the test register meet a first condition;

providing a branch address to a program counter to cause a branch if the contents of the test register meet the first condition; and

modifying the contents of the test register if the contents of the test register meet the first condition.

11. (Amended) The method of Claim 10, further comprising the steps of:

testing a predicate register selected by the conditional ~~branch~~ branch-decrement instruction to determine if the contents of the predicate register meet a second condition; and

inhibiting the step of providing a branch address to the program counter and inhibiting said step of modifying the contents of the test register if the contents of the predicate register do not meet the second condition.

12. (Original) The method of Claim 10, wherein the step of modifying decrements the test register.

13. (Original) The method of Claim 10, wherein the steps of testing, providing, and modifying are all performed during a same execution phase of the microprocessor.

14. (Canceled)

15. (New) The digital system of Claim 1, further comprising:

a register file including a plurality of general purpose registers, each general purpose register capable of supplying an

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operand to a functional unit and capable of receiving destination data generated by a functional unit; and

wherein said conditional branch-decrement instruction designates one of said general purpose registers as said selected test register.

16. (New) The digital system of Claim 15, further comprising:

second test circuitry connected to test a condition of a selected predicate register, and having an output for indicating a condition of the predicate register, wherein the second test circuitry is operable to inhibit the program counter from receiving the branch address and inhibit said step of modifying the contents of the test register if the contents of the predicate register do not correspond to a second condition; and

wherein said conditional branch-decrement instruction designates one of said general purpose registers as said predicate register.

17. (New) The digital system of Claim 16, wherein:

said conditional branch-decrement instruction designates one of said general purpose registers of a predetermined subset of said general purpose registers as said predicate register.

18. (New) The digital system of Claim 1, wherein:

said program fetch circuitry operable to fetch a fetch packet of a predetermined plurality of instructions each first portion of the plurality of pipeline phases starting at predetermined address boundaries; and

said adder circuitry adds said displacement value to said predetermined address boundary of said fetch packet containing said conditional branch-decrement instruction.

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19. (New) The digital system of claim 18, wherein:

said instruction decode circuitry reads a predetermined bit of each instruction to determine an execute packet of instructions capable of execution in parallel on a plurality of functional units, wherein an execute packet may include instructions in two sequential fetch packets; and

said adder circuitry adds said displacement value to said last predetermined address boundary of a second sequential fetch packet if said second sequential fetch packet contains said conditional branch-decrement instruction.

20. (New) The method of Claim 10, further comprising the step of:

storing data in a register file including a plurality of general purpose registers;

recalling data from an instruction designated general purpose register for supplying an operand to a functional unit;

storing destination data generated by a functional unit in an instruction designated general purpose register; and

designating via the conditional branch-decrement instruction one of said general purpose registers as said selected test register.

21. (New) The method of Claim 20, further comprising:

testing a predicate register selected by the conditional branch-decrement instruction to determine if the contents of the predicate register meet a second condition; and

designating via the conditional branch-decrement instruction one of said general purpose registers as said predicate register.

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22. (New) The method of Claim 21, wherein:

said step of designating said predicate register designates said predicate register from a predetermined subset of said general purpose registers as said predicate register.

23. (New) The method of Claim 10, wherein:

said step of fetching instructions fetches a fetch packet of a predetermined plurality of instructions; and

said step of providing a branch address to the program counter adds a displacement value to said predetermined address boundary of said fetch packet containing said conditional branch-decrement instruction.

24. (New) The method of claim 23, wherein:

reading a predetermined bit of each instruction to determine an execute packet of instructions capable of execution in parallel on a plurality of functional units, wherein an execute packet may include instructions in two sequential fetch packets;

dispatching each instruction of each execute packet to a corresponding functional unit in parallel;

said step of providing a branch address to the program counter adds said displacement value to said last predetermined address boundary of a second sequential fetch packet if said second sequential fetch packet contains said conditional branch-decrement instruction.